ABSTRACT OF THE DISCLOSURE

An apparatus and method for a pseudo-dynamic latch are disclosed. A deracer circuit includes a first logic gate configured to receive a data signal from a domino logic circuit and to invert the data signal. A second logic gate is configured to receive the inverted data signal and an inverted select signal and to generate a select signal. Thus, the deracer circuit is configured to prevent the select signal from being high when a precharge edge of a data signal arrives.